Precharacterisation of Si/SiGe Qubit Shuttling Devices at 4 Kelvin

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Abstract:

Semiconductor-based quantum computing continues to attract attention due to their promising scal-ability and the extraordinary technological prospects associated with many-qubit quantum comput-ing. Semiconductor spin qubits in Si/SiGe heterostructure quantum dots have been extensively studied in the past decade. Recent work focuses on achieving robust coupling of the spin qubits across long distances, otherwise known as shuttling. In the context of spin shuttling research, precharacterisation refers to a set of preliminary screening operations on batches of shuttling de-vices with different Si/SiGe heterostructure designs. Conducted at 4 Kelvin, precharacterisation identifies the best suited devices for the 10 mK experiments studying electron charge shuttling and electron spin shuttling. This report presents an overview of the device parameters, the operation details, and the key results of precharacterisation.

Introduction. Silicon-based electron spin qubits have shown promise as a platform for quantum computers. Electron spin af-fords a two-level system required of a qubit via its spin up and down states [1] and maintains long spin coher-ence times due to its low magnetic coupling to external environments [2]. In addition to these advantages, the development of semiconductor electron spin state initial-isation, readout, and control techniques [3–5] and spin qubit gates on the silicon platform [6, 7] make silicon-based electron spin qubits satisfy the DiVincenzo criteria considered necessary for the physical realisation of qubits [8].

The spin qubit programme set forth by DiVincenzo and Loss via electrostatically-defined quantum dots [1] is pursued not only for its feasibility but also its prospect of scalability. The roughly 100 nm size of a single QD spin qubit system and the compatibility of silicon-based qubit systems with industry-scale, silicon nanotechnology infrastructure could lead to surpassing the one-million qubit benchmark necessary to perform major quantum algorithms [9]. Despite these prospects, there currently exists a severe upper limit on the density of spin qubits on a semiconductor chip known as the wiring bottleneck [10] or signal-fanout problem [11]: there is not enough space to accommodate for the networks of qubit control lines connecting qubits to control electronics. The need for transmitting control signals to electrostatic gates to conduct computation and error correction, the need for regular readout of spin states to verify state fidelity, and the requirement for no two qubits to share connection lines [9].

One countermeasure actively being researched is to couple spin states across distances at least a few microns or longer, henceforth referred to as 'spin shuttling' [11].

If spin qubits could be spatially spread out while main-taining their coherence, this will demonstrate increased feasibility of many-qubit silicon quantum computers. Dr. Schreiber's team within the RWTH Aachen Quantum Technology Group focuses on the design, fabrication and measurement of electrostatically defined quantum dot de-vices comprising of metal gates on planar Si/SiGe het-erostructure to achieve spin shuttling. The goal of this report is to describe a subsection of the measurement aspect known as '4K precharacterisation'.

Precharacterisation. The spin qubits are formed from confined electrons in a two-dimensional electron gas (2DEG) formed in a quantum well in the conduction band of a layer of silicon strained between a two, much thicker layers of $Si_{0.7}Ge_{0.3}$ alloy. More specifically, t here i s a channel o f interlacing gates (channel gates) with one single-electron transistor (SET) on each end (left SET and right SET). The SETs are also controlled by gates (top, barrier, and plunger gates). These electrostatic gates fabricated above the heterostructure facilitate the voltage manipulations re-quired for the accumulation and depletion of the 2DEG in the SET and channel, which corresponds to the forma-tion and manipulation of single or few-electron quantum dots.

With applied magnetic fields a nd a dditional voltage pulse signals, the spin-degenerate states of these confined electrons could be separated and manipulated, but this is beyond the scope of 4K precharacterisation. 4K prechar-acterisation focuses on screening for the best devices to conduct the actual spin-shuttling experiments. After the devices are thermally coupled to 4K liquid helium and electrically connected to measurement instruments, spin-

shuttling experiments are recommended only for the devices that could satisfy the following criteria near perfectly or perfectly [12]:

1. SET Characterisation. A 2DEG could be accumulated and a voltage with a stable saturation current could be specified (henceforth referred to as "pinching-off the 2DEG") after sweeping the voltages of the electrostatic gates. Each SET has an associated top gate, barrier gates, and plunger gates. For each subgroup of gates, the ability to pinch-off the 2DEG is verified. The current stability at the pinch-off voltage is verified over a time interval of 60 seconds.

2. Channel Characterisation. A current path could be accumulated through the channel. One SET is biased, and the channel gates are swept un-til some current from the biased SET flows through the channel into the unbiased SET on the other side. Additionally, each channel gate can be swept alone and still facilitate this current flow.

If all subgroups of SET gates and every channel gate could influence t he p otential o f t he 2 DEG, t hen t he de-vice is much more likely to be able to handle the complex voltage pulses used to form single and few-electron quan-tum dots.

Results. Out of 30 devices from 6 different heterostructure de-signs, 3 perfect devices and 7 roughly perfect devices were identified and placed in a queue for the shuttling experi-ments. Other lab members also conducted precharacteri-sation on roughly 60 devices in the previous four months.

In order to make statistical analysis of the performance of each heterostructure design, the data collected for all devices were organised into a .csv file. A plotting pro-gram was written to parse the .csv file entries and yield scatter plots and histograms based on any number of parameters from the following: Heterostructure Batch, Supplier, Design, LSET Pinch-Off Voltage, RSET Pinch-Off Voltage. Two sample plots are shown in Figures 1 and 2.

Concusion. As data for different heterostructure designs accumu-lates, better correlations could be made between a het-erostructure design and some quantity for SET or chan-nel gate performance. The program for parsing the .csv file could be expanded to store any number of quantitative information from any of the precharacterisation tests. Consequently the plotting program could be expanded to accept more axes choices.

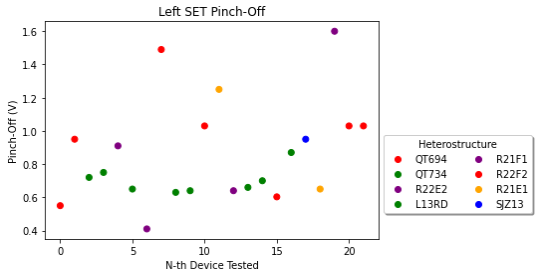

FIG. 1. Scatter plot of the Left SET pinch-off voltages for a sample of devices from a variety of suppliers denoted by colour.

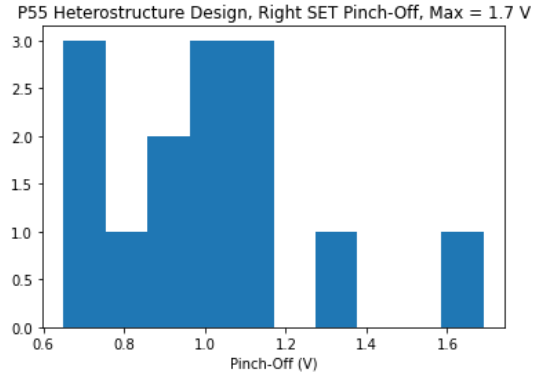

FIG. 2. Histogram of the Right SET pinch-off voltages up to a user-specified maximum voltage and a user-specified heterostructure design of interest.

Although there is not enough data to make conclusive remarks about the strengths and weaknesses of each heterostructure design with respect to 2DEG accumulation and quantum dot formation, this project drastically simplifies the interpretation of data hitherto gathered.

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